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VARIOUS NANO-SCALE TECHNOLOGIES: LOWER HARDWARE COMPLEXITY OF ALU REALIZING UTILIZING FS-GDI APPROACH IN 45nm AND 130nm

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Abstract

Full Swing– Gate Diffusion Input (FS-GDI) approach is power effective approach for realizing the different logic gates. In this research, this approach is utilized for realizing different four ALU design using 45nm and 130nm technologies. Also, the different low power VLSI logic styles and related past works are discussed with considering the 45nm and 65nm technologies for implementing various circuits for studying the technology size impact. The performance of the proposed ALU design is evaluated through power consumption, propagation delay and number of transistors. The variation of the ALU

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performance due to the used 45nm and 130nm technologies has been studied. The simulation is carried out utilizing Cadence Virtuoso simulator. The simulation experiments revealed the energy of the 4-bit ALU reduced by 32% compared to CMOS-based design and area of the digital circuits reducing. Regarding the different nano technologies, 45nm technology provides lower power consumption and delay time deceasing compared to ALU unit by 130nm technology. The presented approach of low hardware complexity achieves simplicity of the required ALU hardware through reducing the number of transistors.

Keywords: 4-bit ALU, power efficiency, 65nm technology, 130nm technology, FS-GDI, hardware complexity.

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1. Introduction

Due to the growth in technology and mobile applications, power consumption considered one of the fundamental limits in portable systems and high-performance microprocessors has become a primary focus of attention in VLSI digital design. In high-performance systems, power is the limiting factor for a further increase in clock speed and circuit density, due to the difficulties of conveying power to circuits and removing the heat that they generated. In portable battery-operated devices, such as cell phones, bio-medical devices, sensor networks, etc., power consumption is critical since it determines the lifetime of the battery. It also affects the device size, cost and weight [1-8].

The increasing demand for low-power VLSI achieved at different design levels, such as the architectural, circuit, and the process technology level. At the circuit design level, considerable power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters dominating power dissipation such as switching capacitance, transition activity, and short circuit currents are influenced by the chosen logic style. Different performance aspects become important depending on the application, the kind of circuit to be implemented, and the design technique used. The logic style used in logic gates basically influences the

speed, size, power dissipation, and the wiring complexity of a circuit. The circuit delay is determined by the number of transistors in series, transistor sizes, and wiring capacitances. Circuit size depends on the number of transistors, their sizes and on the wiring complexity [8-15].

Power dissipation is determined by the switching activity and the node capacitances which in turn is a function of the same parameters that also control circuit size. Finally, the wiring complexity is determined by the number of connections and their lengths and by whether single rail or dual rail logic is used [16].

All these characteristics may vary significantly from one logic style to another and thus make the proper choice of logic style critical for circuit performance. Robustness with respect to voltage and transistor scaling as well as varying process, working conditions and compatibility with surrounding circuits are important aspects influenced by the implemented logic style [17]. Low power logic styles are discussed in the next section.

The various versions of GDI approach is discussed in Section 4. Section 5 presents the proposed work description.

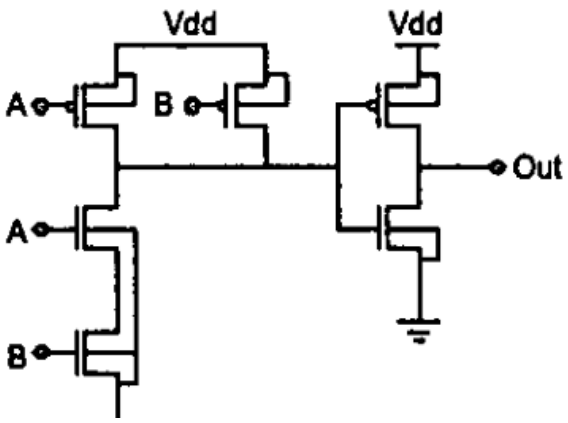
2. Contributions and Motivation

The ALU is vital unit in the data processing and implementation the different electronics circuits of the DSP, image processing, data encoding, data decoding, encryption, decryption processes and another data processes. Hence, with presenting efficient power ALU unit, the overall circuits of the data/image processing can be reduced. The FS-GDI approach is used for realizing the proposed ALU design for improving the delay time and the power efficiency. There are more than proposed design has been presented in this research paper. The proposed designs of the ALU are implemented by the low power FS-GDI and the traditional CMOS approaches with 45nm and 130nm technologies.

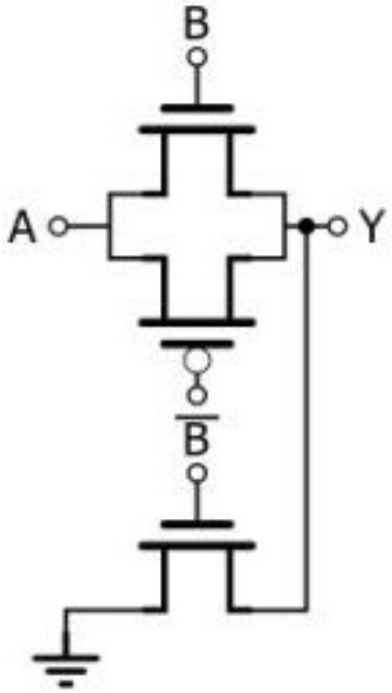
The performance comparison between the different circuits design with technology levels considered. In this comparison, the previous circuits design utilizing 45nm technology is re-built using 65nm technology. The consumed Power (P), Delay time (D), and Power Delay Product (PDP) are employed to evaluate the performance of the proposed ALU design. The proposed design and simulation experiments are performed by Cadence Virtuoso simulator.

3. Low Power VLSI Approaches Overview

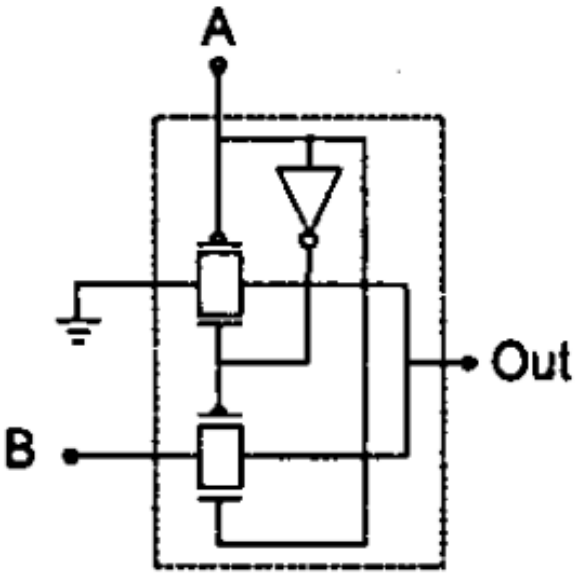
The different styles of the VLSI are presented in this section. In the following, the different approaches advantages and disadvantages are discussed. In Figure 1, the AND logic gate realizing using the different approaches [18-25].



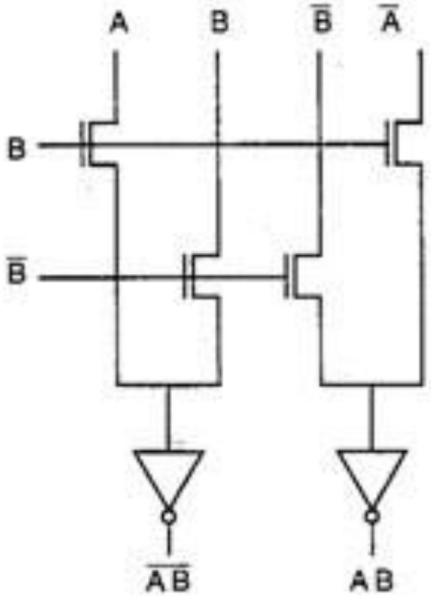
(a) CMOS AND gate



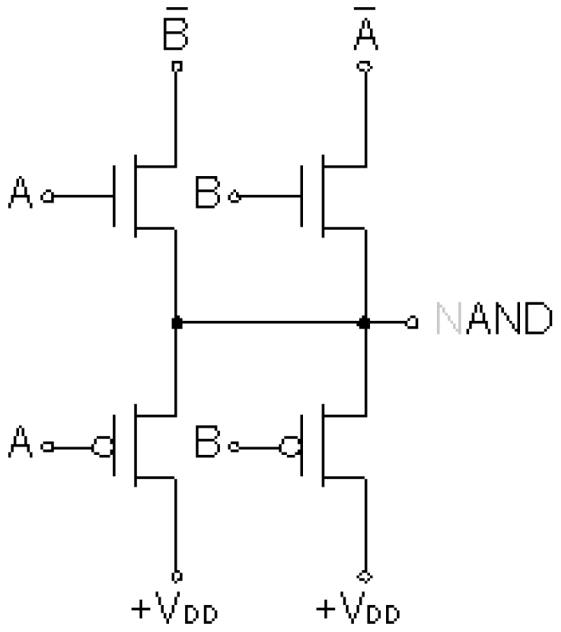
(b) AND gate-PTL



(c) AND gate-TG



(d) NAND/AND gate-CPL



(e) AND gate DPL

Figure 1. Different traditional approaches for realizing AND logic gate.

The complementary symmetry metal-oxide-semiconductor CMOS is the most popular approach, it has several advantages such as, low noise margin, high speed, low power, easy to develop, common in most chips design of VLSI. Also, it suffers some problems such as, high power dissipation, large number of transistors/area, long delay time, power consumption high. The second common approach is the Pass Transistor Logic (PTL), it is popular as CMOS approach, its features as decreased silicon area, speed, reduced power consumption, slower at reduced power, significant power dissipation. The third approach is the Transmission Gate (TG), its feature is less transistor for implementing complex gates, PMOS and NMOS combination avoid noise margin, power dissipation, switching, require control, limited TG cascade. The fourth approach is the Complementary Pass-Transistor logic- (CPL), (N-MOSFET approach), its advantages is high speed, low i/p capacitance and easy to implement complex logic by NMOD net. It is drawbacks is drop in threshold voltage,

static power consumption and delay increases with long pass-transistor chains. The Double Pass-transistor Logic (DPL) approach is the modified of CPL approach, it has some advantages as well-balanced input capacitance No drop voltage, no need buffers, full swing and low power, its main problems are large area and inverters need [25-30].

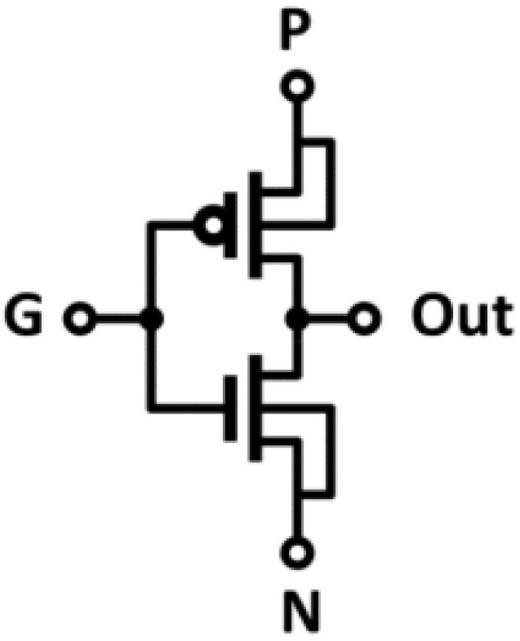
4. Versions of Gate Diffusion Input Technique (GDI) Approach

A long fourteen years, Morgenshtein et al. presented the GDI approach for low power VLSI implementing. In 2001, 2010 and 2014, the original cell of GDI, modified GDI and Full Swing GDI have been presented, respectively by Morgenshtein. Gate diffusion input (GDI) is a new low power technique using small silicon chip area for digital VLSI design compared to another logic style proposed in [8, 9]. This approach aimed to improve the power consumption and area as well as propagation time of the logic gates implementing compared to the traditional approaches [6, 31-33].

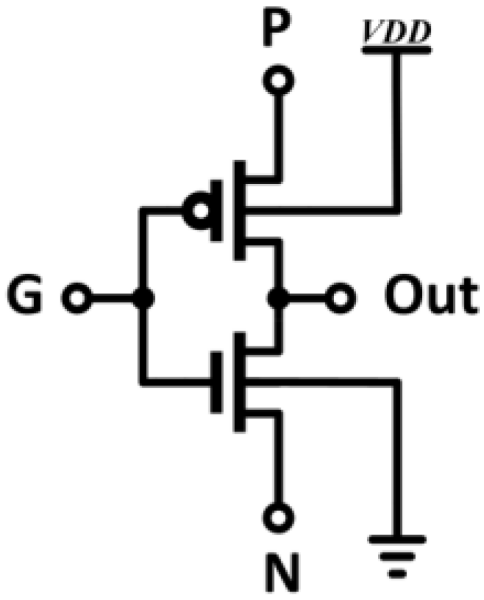
In 2001, the GDI approach was invented, it allowed complex gate implementing by two transistors. This method is suitable for the design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques) as shown in Table 1 [8].

Table 1. Transistors count between GDI and CMOS for various functions

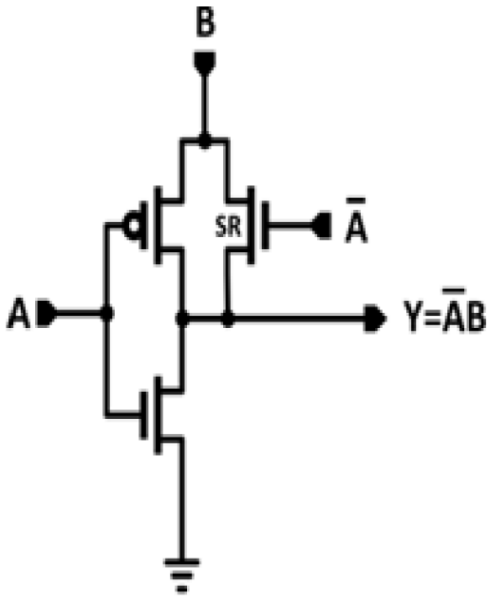
Different realized function	CMOS approach	GDI approach
F1 = $\overline{A}$B	6	2
F2 = $\overline{A}$ + B	6	2
OR	6	2
AND	6	2
NAND	4	4
NOR	4	4
MUX	12	2
NOT	2	2



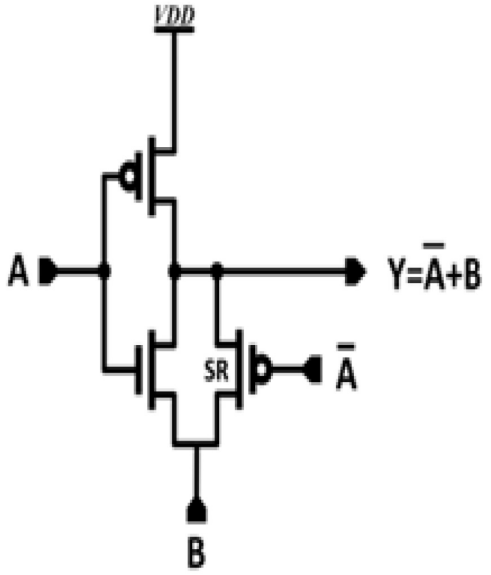
(a) Original GDI cell



(b) Modified GDI cell



(c) FS-GDI cell (Last version of GDI approach)



(d) NOR gate FS-GDI

Figure 2. Cell of GDI approach developing during 2001-2014.

Figure 2 shows the GDI approach versions from 2001 to 2014. Figure 2(a) gives the original cell of GDI, Figure 2(b) presents the modified cell, while the last version of GDI approach is shown in Figure 2(c), and Figure 2(d) gives the XOR implementation by the FS-GDI approach. Using GDI technique allowed improvement in power consumption, propagation delay and area of VLSI digital circuits compared to CMOS and pass transistor logic (PTL) techniques. PTL and GDI both suffered from reduced voltage swing at their outputs due to threshold drops. Problems of the first GDI cell are solved by Morgenshtein [11]. He proposed Full Swing GDI (FS-GDI) based on a single swing Restoration Transistor (SR) as an alternative to another method. SR transistor ensures full swing operation [35]. The logic gates such as AND, OR, and XOR gates can be implemented with full swing operation can be achieved but with increasing the transistor count from 2 to 3 compared to the original GDI design. So, Shoba proposed a new design of AND, OR, and XOR logic gates based on full swing GDI technique, which are used to implement three designs of full adder [39].

However, the three full adders are successfully realized using full swing gates with a significant improvement in their performance [40-42].

5. The Proposed Work Discussion

Due to the importance of ALU unit in DSP and image processing applications, this research presents efficient ALU design based on FS-GDI approach using 65nm and 130nm technologies. This proposed ALU design achieves low power consumption, short propagation time delay and area reduction through decreasing the required number of transistors. On the other hand, the low power VLSI fabrication in the nano size technologies plays role in realizing low power electronic circuits. In this research, four design of ALU units are presented using the efficient FS-GDI approach within different fabrication technologies '45nm & 130nm technologies'. The amount of power consumption, delay time, no. of transistors, and energy product are employed as a metrics for evaluating and analyzing the performance of the proposed ALU design compared to the traditional CMOS approach. Also, the ALU performance with the different technologies is considered in the simulation results evaluation and analysis. there are wide comparison between the presented design and the previous related works where the technology levels (45nm and 45nm) and implementing approaches are considered [30].

6. Past Related 45nm Technology and 45nm Technology Testing

In this section, simple nano size technology of VLSI definition is presented. Also, in this section, the performance of 45nm and 45nm technologies has been discussed by re-building the previously published 45nm circuits by different approaches of VLSI fabrication but using 45nm technology.

6.1. Nano technology in VLSI fabrication overview

Due to the rapid and huge advances in the wireless communications and its applications in the different fields such as the wireless sensor networks and wireless body area networks, the very lower power consumption electronics needs became highly required. On the other hand, almost, the power consumptions is related to the area or the volume of the electronic device. The nano-size VLSI fabrication is a perfect way for reduction the area and the required consumed power [34].

Firstly, the meaning of 180nm, 90nm, and etc. technology, means the numbers represent the minimum feature size of the transistors PMOS or NMOS on the chip. The minimum feature size means that during the fabrication process of a transistor, how closely the transistors can be placed on a chip to be used for various purposes. With the smaller size, the larger number of smaller transistors can be fabricated/collected on the same chip, these chips occupy low area/volume, faster, high power efficient. These nano-size technologies have some disadvantage such as the leakage power consumption is high due to sub-threshold leakage increasing and decreased noise margin. As shown in Figure 3 the advance in technology node process following Moor's law [35].

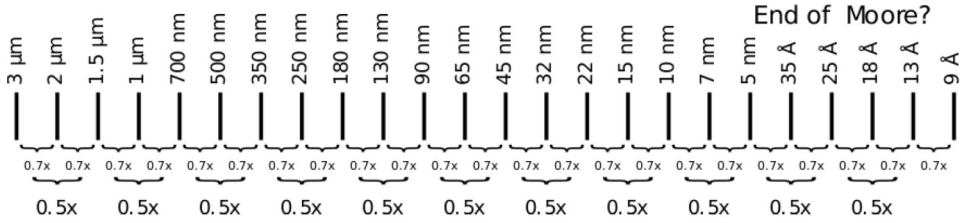


Figure 3. Technology node CMOS process.

6.2. Impact of 45nm & 45nm technologies

In this subsection, the 45nm and 45nm are chosen to study the impact of technology on circuit performance in terms of power consumption, delay, and PDP.

In [35], full adder design has been presented using 45nm technology and CPL approach as shown in Figure 4. This design in Figure 4 is re-build by Cadence Virtuoso simulator by the same approach and 65nm technology. The presented design of CPL full adder which tested in [35] by using 45nm technology and approach process the result is consuming power 2.68μW, delay 38.8 pS and PDP 103.9 aJ and when tested in 45nm consume power 7.5μW, delay 63.8 pS and PDP 478.5 aJ [14].

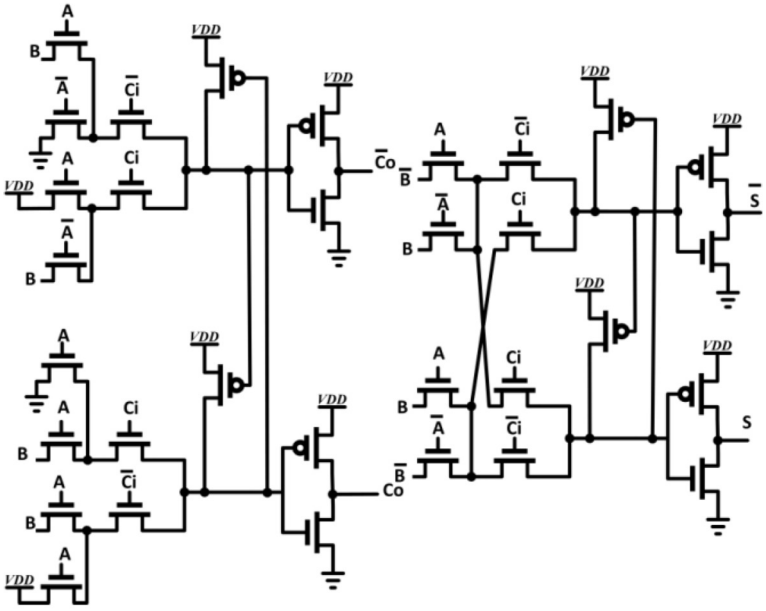


Figure 4. Full adder designed by CPL technique.

Figure 5 presents design of C-CMOS full adder which tested by using a 45nm technology and CMOS process the result is the consuming power 0.975μW, delay 46 pS and PDP 45 aJ and when tested in 45nm consume power 7μW, delay 45.75 pS and PDP 460.25 aJ [13].

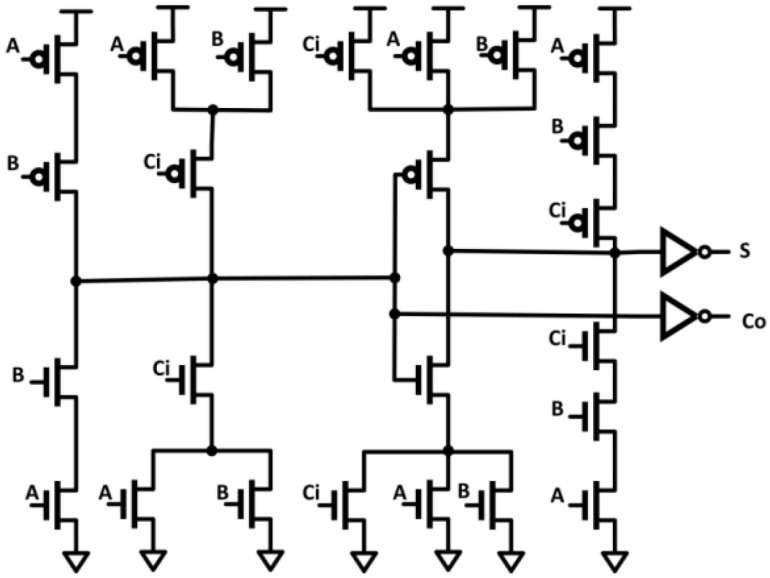


Figure 5. Full adder designed by C-CMOS technique.

Figure 6 presents the design of a hybrid full adder which tested by using a 45nm CMOS process the result is consuming power 1.613μW, delay 35 pS and PDP 56.8 aJ and when tested in 45nm consume power 6.4μW, delay 43 pS and PDP 275 aJ.

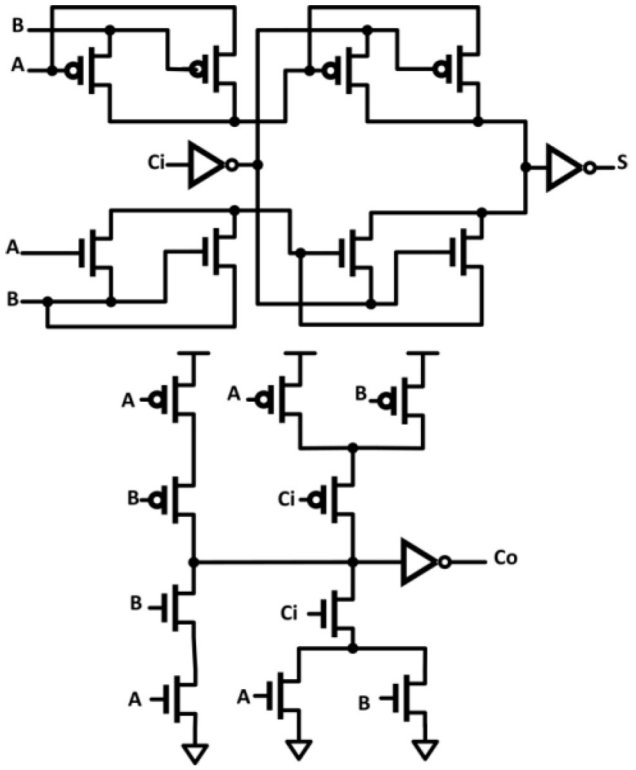


Figure 6. Full adder designed by hybrid technique.

Table 2 presents the simulation results of 1-bit full adders at the 45nm technology process compared to 45nm technology used in [35].

Table 2. Simulation results of different full adder circuits in TSMC 45nm CMOS and 45nm process technology

Realizing approach	Technology level							
	45nm				45nm			
	P (μW)	D (pS)	PDP (e-18J)	No. of T	P (μW)	D (pS)	PDP (e-18J)	No. of T
CPL [8, 14]	7.5	63.8	478.5	38	2.68	38.8	103.9	38
C-CMOS [13]	7	65.75	460.25	28	0.975	46	45	28
FS-GDI Design 1 [36]	6.3	45	283	18	0.97	37.8	35.1	18
FS-GDI Design 2 [36]	6.6	41	270	23	1.14	26.9	30.6	23
Hybrid-FA [39]	6.4	43	275	18	1.613	35	56.8	18

In this subsection, the impact of the (nano) size of VLSI fabrication technology has been studied by re-build the previously published 45nm circuits utilizing which we own 45nm technology. As cleared in the tabulated results, there wide variation between these two technologies in the consumed power more than the variations in the propagation time delay. In this comparison, the number of transistors is the same due to utilizing the same approaches for realizing the circuits for clearing the really impact of the size in VLSI fabrications [36-38].

7. The Performance of Proposed 4-bit ALU Designs by FS-GDI

In this section, there are two designs for the ALU presented each ALU designed using 2 to 1 mux , 4 to 1 mux and two different full adders implemented using GDI technique in [28], as follows:

7.1. FS-GDI based: Proposed ALU Designs 1 (45nm)

The proposed design of the 4-bit ALU consists of 4 stages; each stage is a 1-bit ALU, which consists of two 2 to 1 multiplexers, two 4 to 1 multiplexers, one full adder cell and an inverter. The full adder used in

this design implemented using the full-swing AND, OR, and XOR gates along with multiplexers, as shown in Figure 7, The Sum and C_{out} expressions are represented in Equations (1) and (2), respectively.

$$Sum = A \oplus B \oplus C_{in}, \tag{1}$$

$$C_{out} = \overline{C_{in}}(A.\ B) + C_{in}(A + B). \tag{2}$$

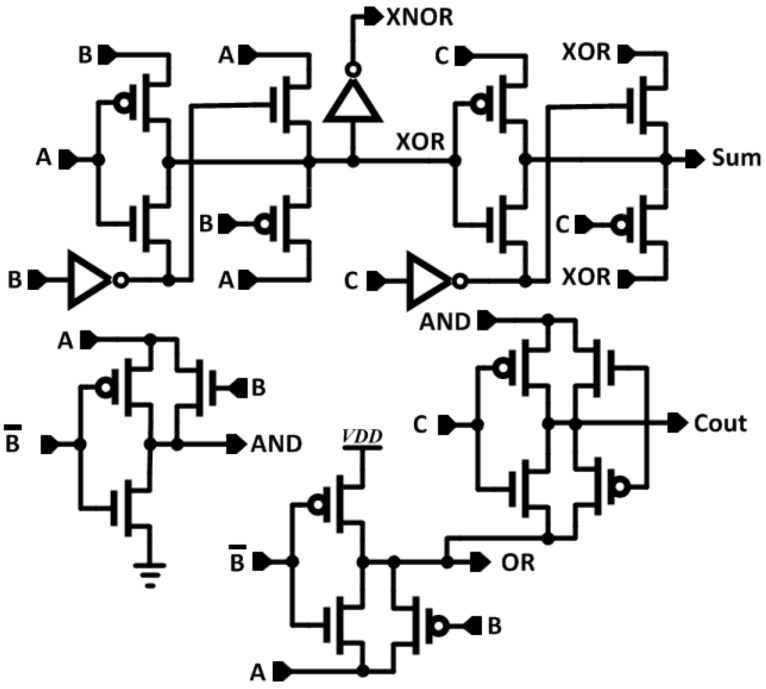


Figure 7. FS-GDI based full adder used in ALU Design 1.

This adder used to generate the arithmetic operations and to generate the logic operations with the help of the logic gates building the adder itself and an inverter gate added to generate the XNOR function. This adder is used to generate both the arithmetic and logic operations, that saves large area of the ALU design due to the reduced transistors which are used to generate logic operations.

The Full-Swing GDI (FS-GDI) design compared to the CMOS counterpart in terms of power consumption, delay, energy, and transistor count. Simulation results of the full adder using FS-GDI and the conventional CMOS logic are shown in Table 3.

Table 3. FS-GDI full adder and logic circuit compared to CMOS

Utilized Approach	Realized Circuits	Performance Metrics			
		P(μW)	D(pS)	No. of Transi.	E (e-18J)
CMOS	F. A + Logic	1.996	37	54	73.85
FS-GDI	F. A + Logic	2.097	13.1	24	27.47

The simulation results of the FS-GDI full adder and logic circuit indicates that the propagation delay and energy reduced by 64.6% and by 62.8%, respectively, while using 55% fewer transistors compared to the conventional CMOS design, however power increased by 4.8%. Simulation results of the 4-bit ALU using FS GDI technique and compared to the conventional CMOS design are listed in Table 4.

Table 4. Simulation results of the 4-bit ALU Design 1

Utilized Approach/Proposed Units	Performance Metrics			
	P(μW)	D(pS)	No. of Transi.	E (e-18J)
4-bit ALU Design 1 using CMOS	33.85	155.6	540	5267
4-bit ALU 4-bit ALU Design 1 using FS-GDI	27.11	69.8	286	1892.27

The analysis and simulation results of ALU Design 1 indicates that the power consumption improved by 20%, propagation delay by 55% and total energy reduced by 64% while using 47% fewer transistors compared to the conventional CMOS design.

7.2. FS-GDI based: Proposed ALU Design 2 & 3 (45nm)

In this subsection, two another proposed 4-bit ALU unit with the same previous subsection except the proposed ALU 3 & ALU 4 use Full Adders previously presented in [39, 40] The results of these ALU units are tabulated in Table 5.

Table 5. Proposed ALU Designs 2 & 3 performance comparison

Proposed ALU 3 & 4 FS-GDI Approach	Performance metrics			
	Power (μW)	Delay (pS)	Transistor count	Energy (e-18J)
Design 2 16T full. A in [40]	26.78	54.4	286	1456.83
Design 3 15T F. A in [41]	28.09	68.5	282	1924.16

As presented in the conclusion Design 2 outperforms Design 1 as it reduced delay time by 22.3% a slight increase in transistor count and power consumption (8 T & 390μW, respectively).

7.3. Analysis of simulation results

As shown in Table 6, Design 3 reduced power consumption by 2.6% (720μW), while increasing delay by 0.33% (0.18pS). Energy improved by 2.3% and reduced transistor count (8 transistors less) compared to ALU Design 2 therefore Design 3 is slightly better than Design 2. In Design 4, power consumption increased by 2.1% (590μW), and increased delay by 26.33% (14.3pS), the energy increased by 29% and reduced transistor count (4 transistors less) compared to ALU Design 2. In conclusion among the 4 designs, Design 2 & 3 both suitable for the proposed ALU, furthermore Design 3 is slightly better. As shown in Table 6, the last presented ALU design provides lower hardware complexity, it consists of 282 transistors only.

Table 6. Proposed ALU Designs 1, 2, and 3 comparison and with respect to the approach

Proposed ALU Design (1-4)	Performance Metrics			
	Power (μW)	**Delay (pS)**	**Transistor count**	**Energy (e-18J)**
CMOS proposed ALU design 1	33.85	155.6	540	5267
FS-GDI proposed design 1	27.11	69.8	286	1892.27
FS-GDI proposed design 2	27.5	54.22	294	1491.05
FS-GDI proposed ALU design 3	26.78	54.4	286	1456.83

7.4. Comparing 45nm & 130nm technology

In addition to 45nm technology, Design 2 implemented in 130nm technology to compare the two technologies. The circuits were designed using 130nm TSMC CMOS process, The simulations were done using the SPECTRE based Cadence Virtuoso simulator with a power supply 1.8V, and a frequency of 125MHz, the size of PMOS is twice of the NMOS transistor $(W/L)_P$ = 300nm/130nm and $(W/L)_N$ = 150nm/130nm for best power and delay performance.

The delay is measured by accounting the time taken from 50% of the input voltage swing to 50% of the output voltage swing for each transition, the maximum delay is treated as the worst-case delay. The design compared in both processes in terms of power consumption, delay, energy as list in Table 7.

Table 7. ALU Design 2 with respect to technology level comparison

nm Technology	Proposed ALU Design 2 Performance Metrics			
	VDD	**D(pS)**	**P(μW)**	**PDP (e-18J)**
45nm Technology	1.2v	27.5	54.22	1491.5
130nm Technology	1.8v	133	91	12103

So, based on the results of metrics performance of proposed design ALU with different technologies as shown in Table 8, it clears the impact of VLSI size fabrication technology. The consumed power metric is impacted more than the delay as shown in Table 8.

Due to the limitations of the Cadence Virtuoso simulator, this research paper is restricted to cover the 45nm and 130nm technologies only. The results of comparisons in Table 2 and Table 8 prove the performance metrics variations between the 45nm and 130nm technologies are wide compared to the 45nm and 45nm technologies.

This research work presents four efficient proposed ALU design as shown in the previous sections utilizing the power efficient VLSI approach which are the FS-GDI approach. The proposed units need low power that may help for implementing more efficient power electronics circuits, lower power Data Signal Processing (DSP) and lower power wireless devices.

In the near future work, simple data protection codes realizing by the FS-GDI will be designed and implemented, for implementing, efficient power, low hardware complexity error control techniques.

8. Conclusion

In this research paper, simulation comparison between the different nano size technologies, it considered the 45nm, and 130nm technologies using Cadence Virtuoso simulator. This comparison clears the impact of size on the performance of the implemented circuits. Also, the paper presents an efficient approach for raising the power efficiency of the data and image processing as well as the power efficiency of the mobile systems. It proposed multi- efficient design for the ALU unit using the FS-GDI approach. It also presents description the different VLSI approaches and wide previous related works survey. The 4-bits ALU designed in 45nm and 130nm CMOS processes using the full-swing GDI technique and simulated using the Cadence Virtuoso simulator. Four

designs for the ALU were presented in Design 1: Results showed the advantages of the proposed ALU design in comparison with conventional CMOS design in terms of power consumption, propagation delay, and transistor count. Hence the energy of the 4-bit ALU reduced by 64% compared to CMOS based design, while using fewer transistors only 286 transistors. In Design 2; delay time of the 4-bit ALU reduced by 22.3% compared to the ALU Design 1, while maintaining full-swing operation. Hence the energy of the 4-bit ALU reduced by 21.2%. Design 2 consists of 294 transistors; both designs operate under 1.2V supply voltage and frequency of 125MHz. Based on the results, it can be concluded that the proposed 4-bit ALU designs are suitable for low energy, lower hardware complexity and high-speed VLSI applications.

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